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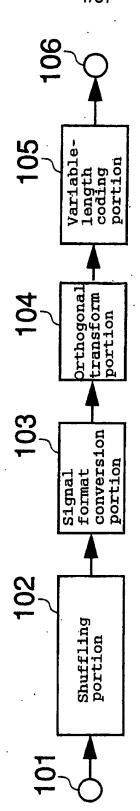
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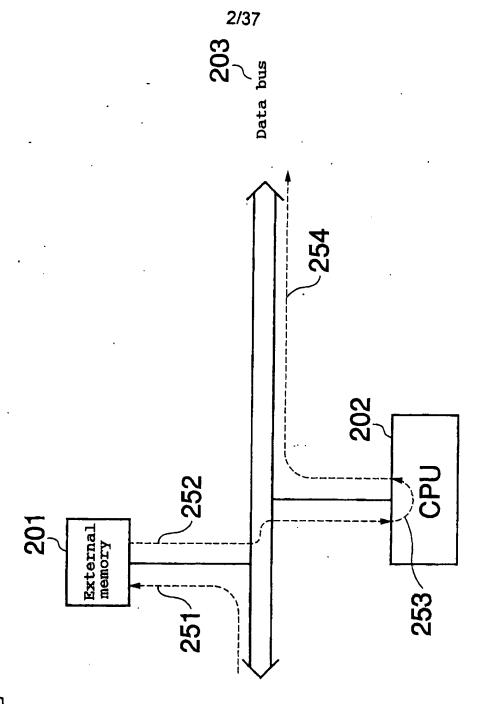
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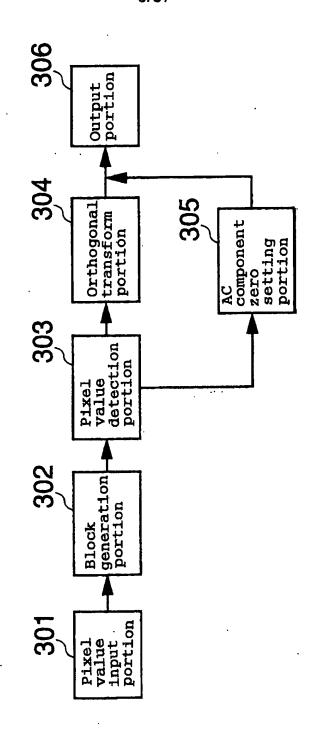
Fig. 1



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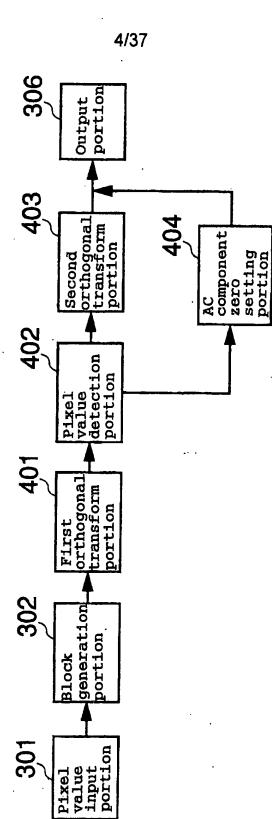
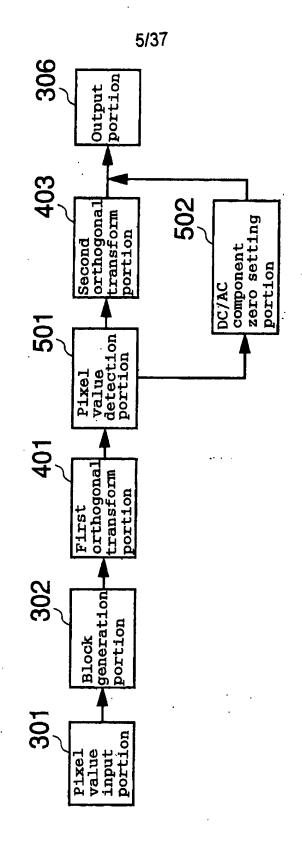


Fig. 4



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Fig. 6

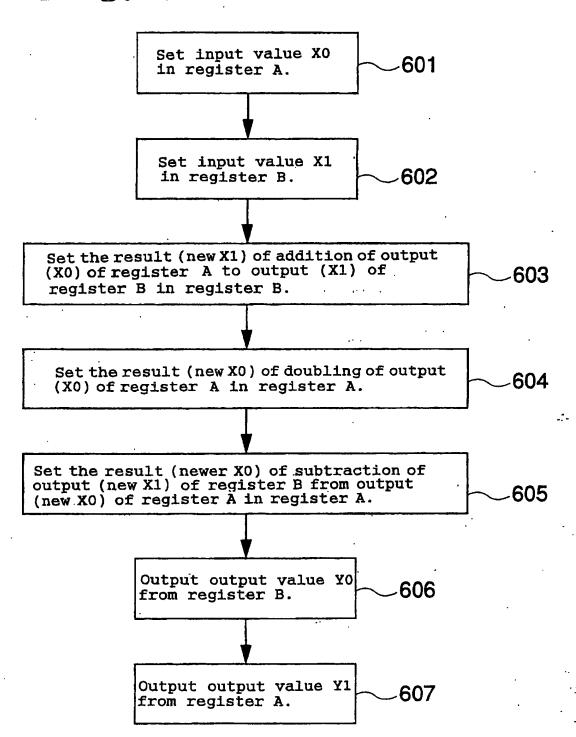


Fig. 7

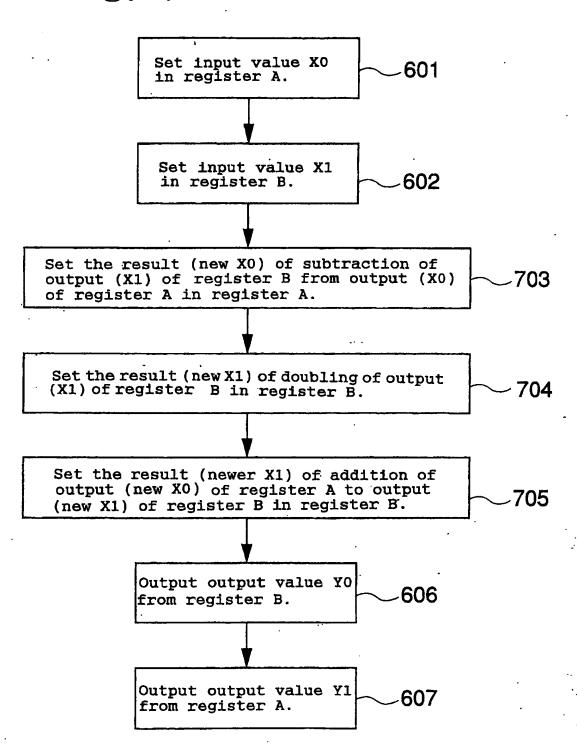


Fig. 8

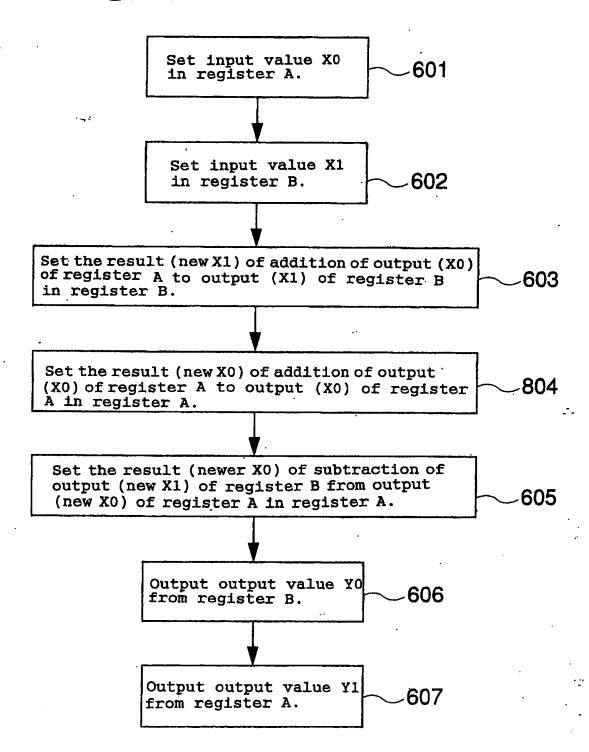


Fig. 9

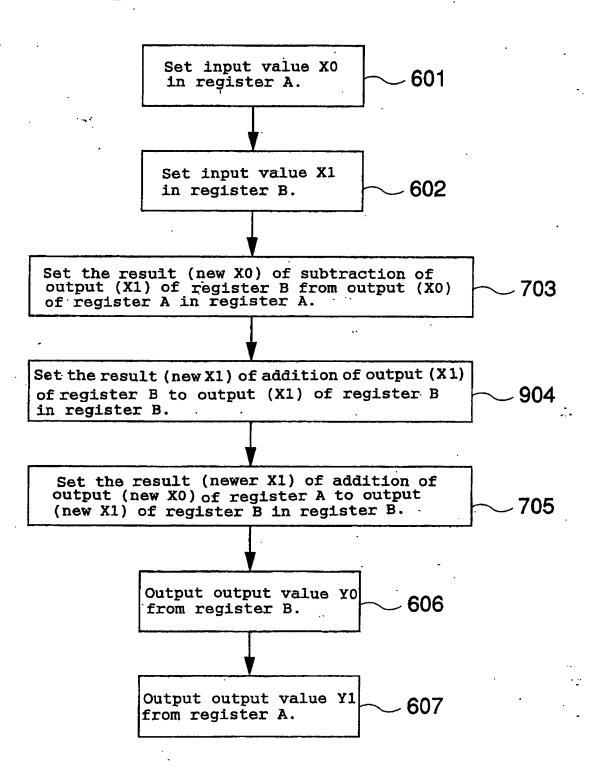


Fig. 10

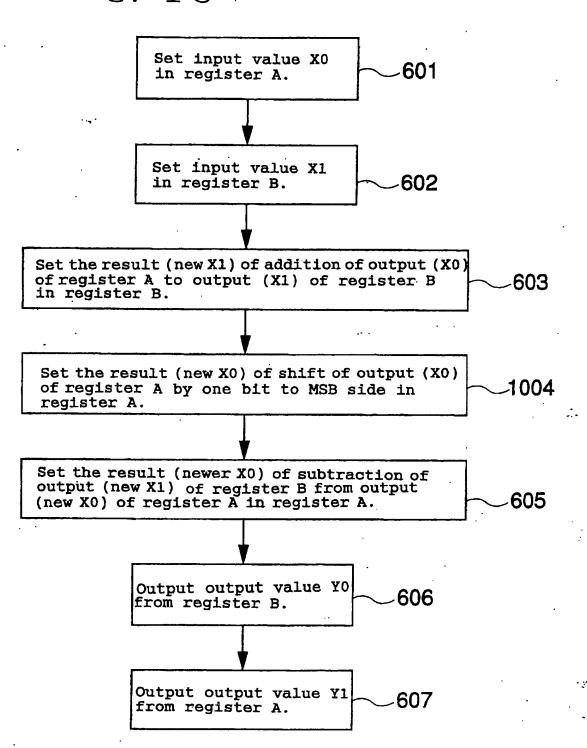


Fig. 11

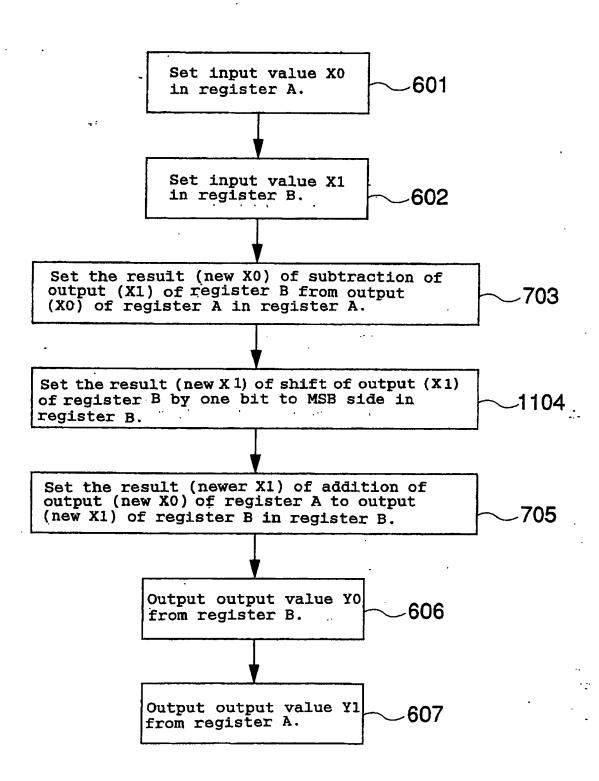
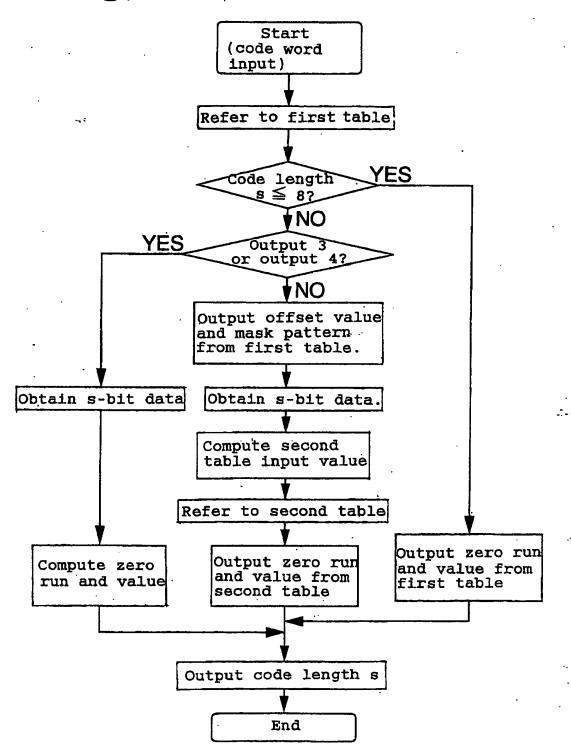


Fig. 12



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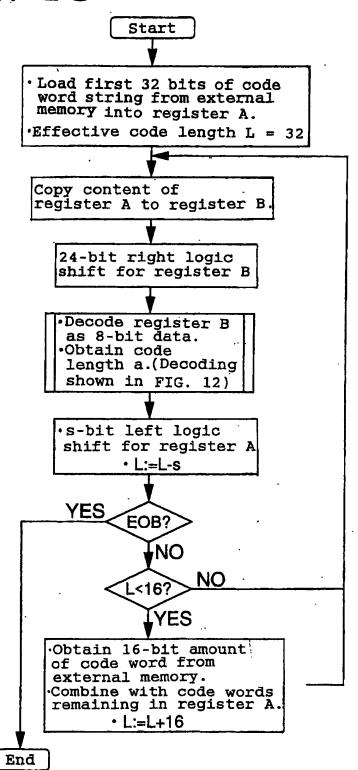
<Zero run is computed from code word.> > (code length, mask pattern, offset) < 13/37 Output 4 (code length, zero run) (code length, zero run, value) Output 3 (code length, value) Output 2 Output 1 13,31,96) (3,0,1)9,31,0 (8,0,11(13,0)(16,0)(5, 1,First table Input (8-bit code) (00000000) (01111100)11100000) (11111110)11011111 (11111011 11111111

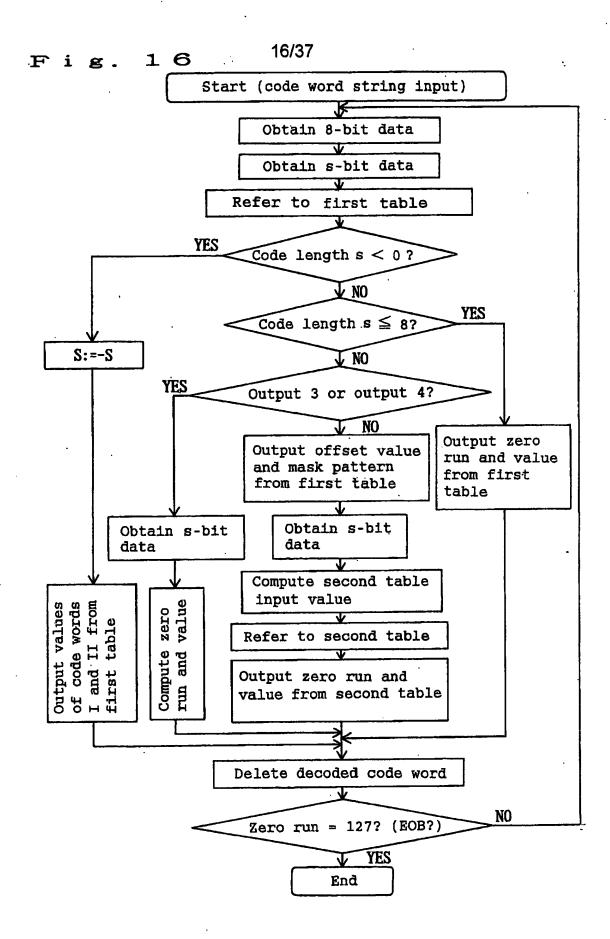
Fig. 13

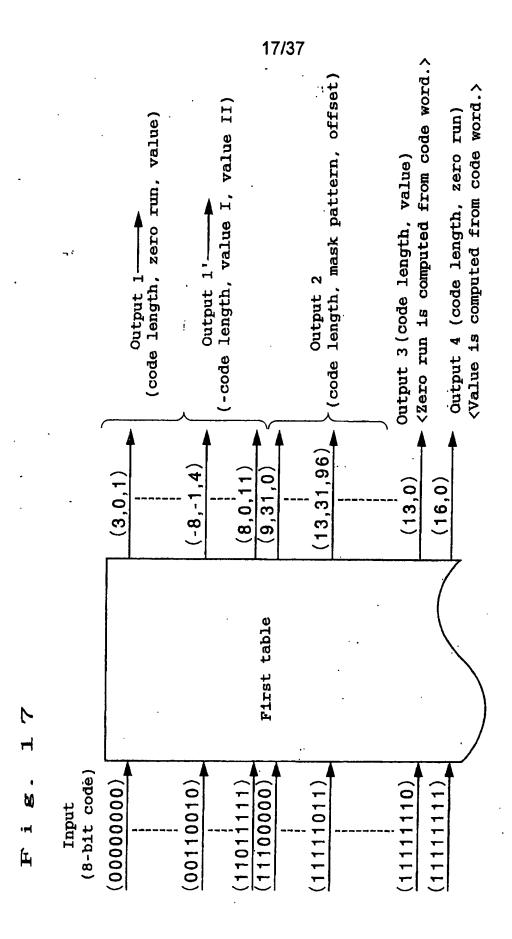
Fig. 14

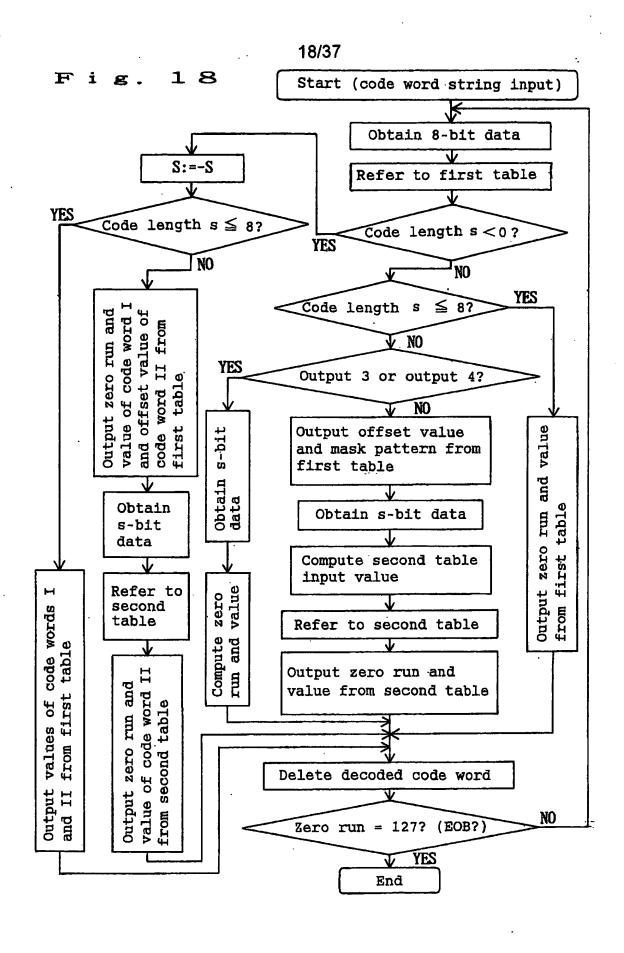
First	table	e output	Code word to be obtained	Second table							
Code	Mask patter	Offset	Masked value (f)	Input address (f + t)	Zero run	Value					
9	11111	0	1110 00000 1110 00001	0	7 7	-1 -1					
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•					:						
	•		11110 11110 1111	62 63	0	22 -22					
11	1111	64	1111100 :0000 :	64 :	5 :	3 : :					
12	1111	80	1111100 1111	79 80 :	1 6 :	3 :					
			11111010 1111	: 95	5	: 0					
13	11111	96	11111011 00000	96 97	7 7 :	2 -2 :					
			11111011 11110	126 127	1	17 -17					

Fig. 15

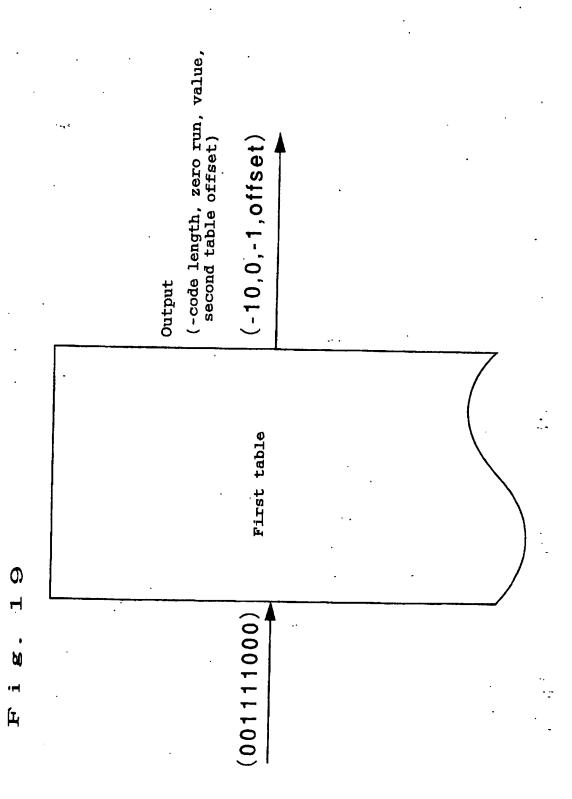




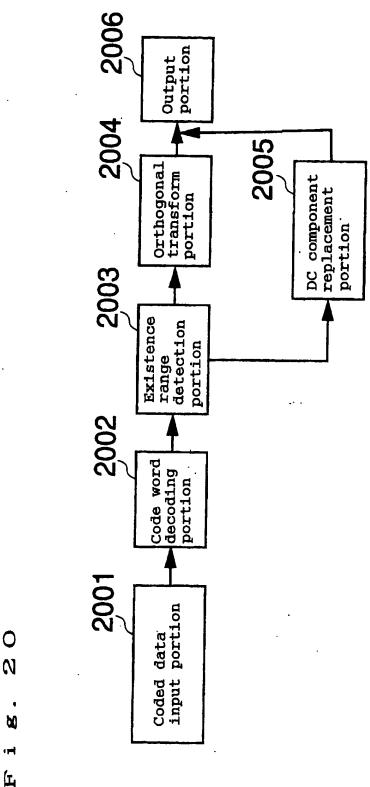




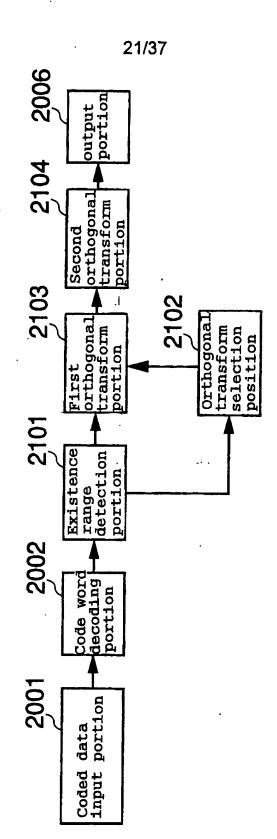




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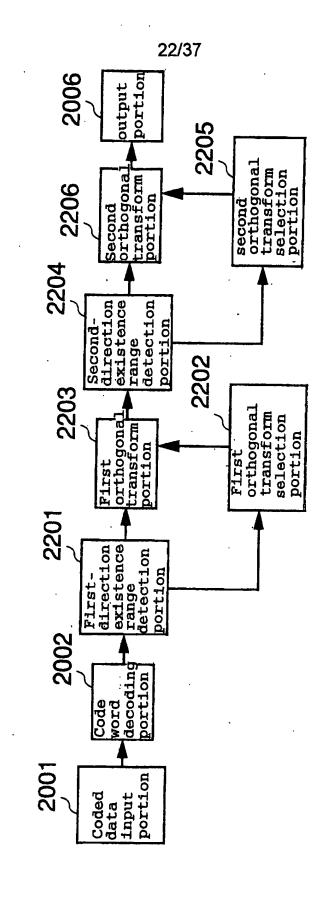


Fig. 22

23/37

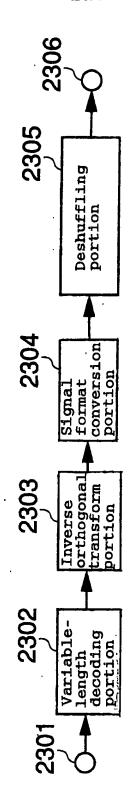
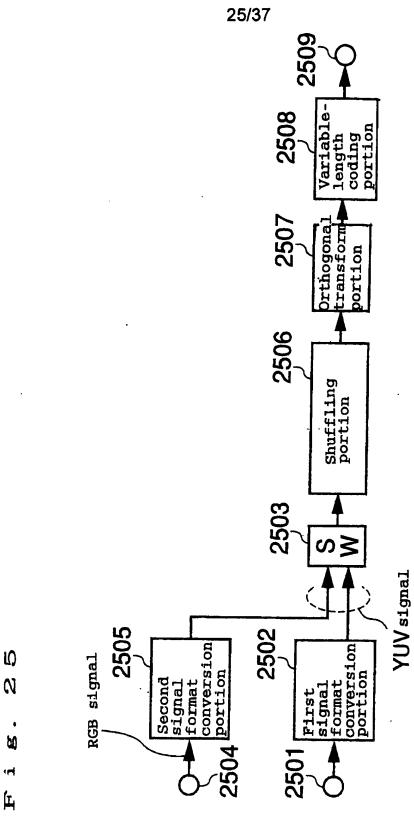
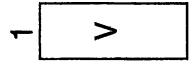


Fig. 23

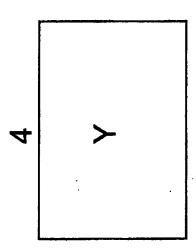
203 203 Data bus -2451 202 CPU External memory

Fig. 2









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Fig. 27

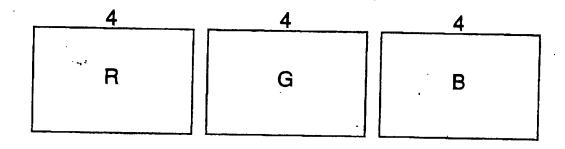
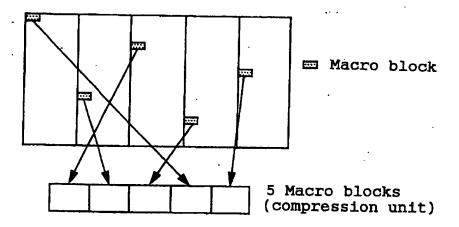


Fig. 28



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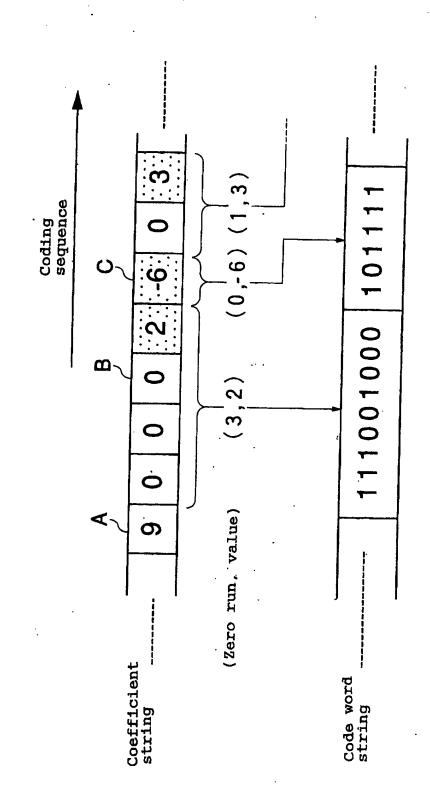


Fig. 30

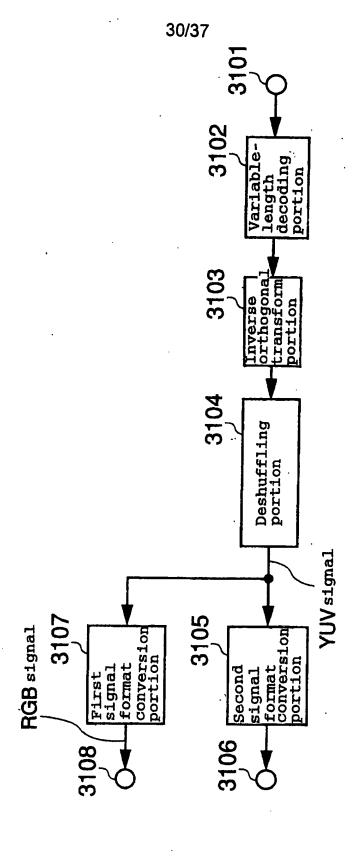
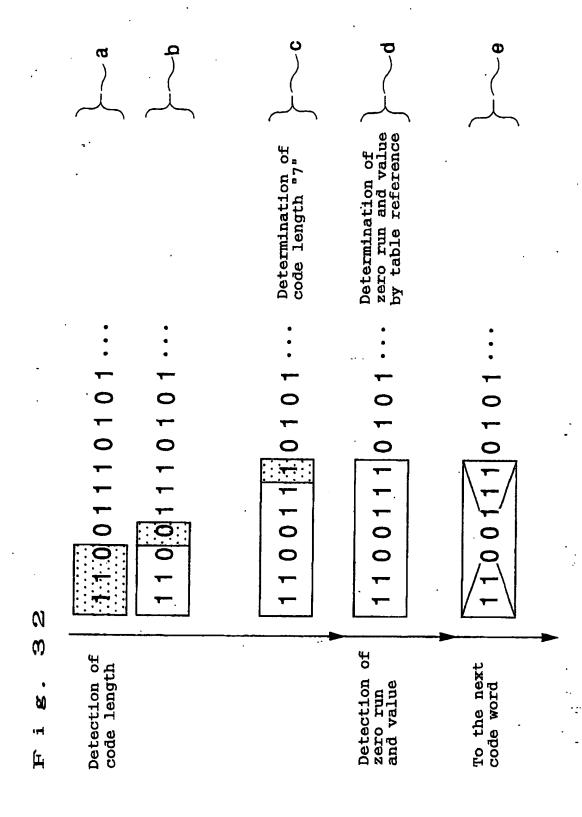


Fig. 31

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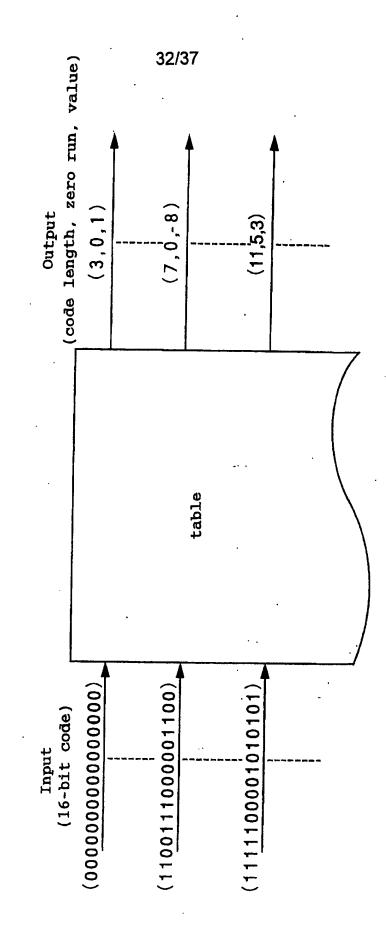
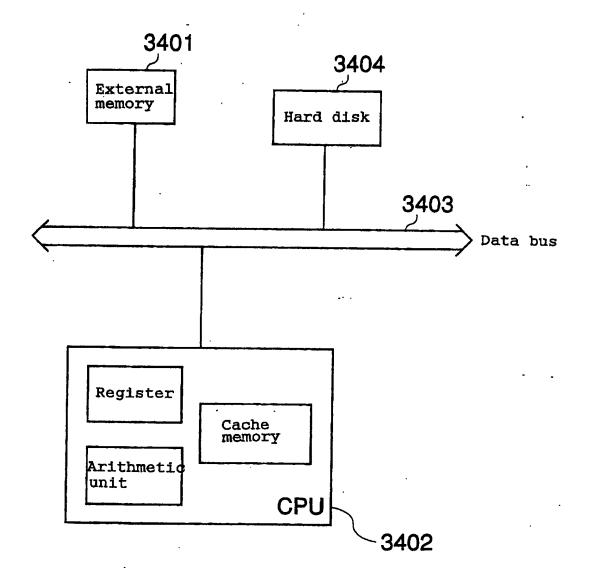
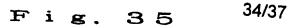


Fig. 33

Fig. 34



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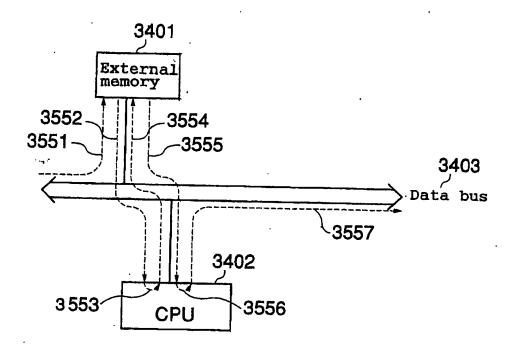
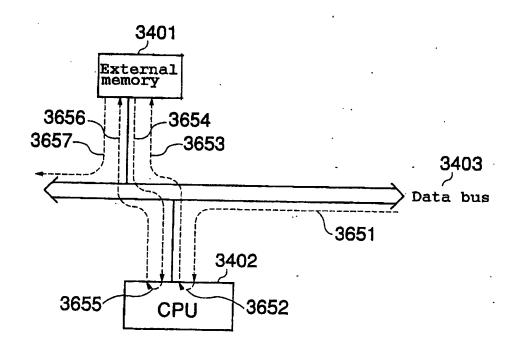


Fig. 36



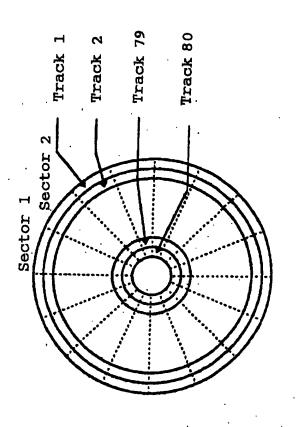


Fig. 37(a

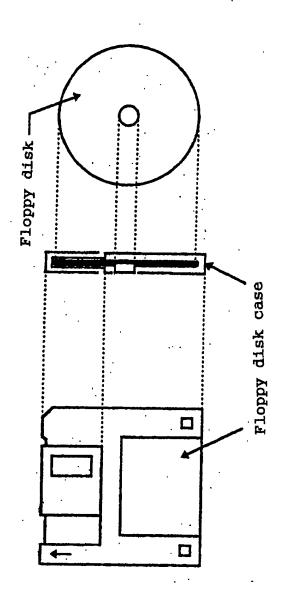


Fig. 37(b)

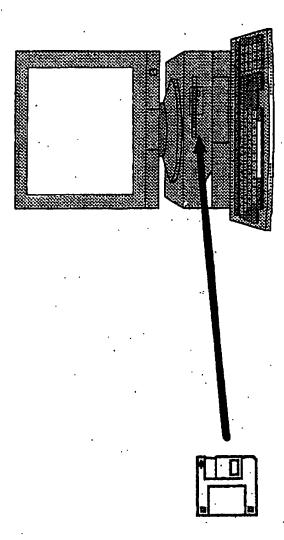


Fig. 37(c)